WHAT IS CLAIMED IS:

1. A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and a closed end within the body of the substrate, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the substrate; and

(b) annealing the trench to:

(1) reduce the number of defects in the trench created during the step of forming, and

(2) to round corners at the open and closed ends of the trench.

2. The method of claim 1, wherein the step of annealing is performed using hydrogen gas.

3. The method of claim 2, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

4. The method of claim 1, wherein the step of forming the trench, is performed using an anisotropic etch.

5. The method of claim 4, wherein following the annealing step, the width of the trench away from the rounded ends, remains substantially the same as the width prior to the annealing step.

6. A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and by a closed end within the body of the substrate, the method comprising the steps of:

(a) providing a substrate;

(b) growing a masking layer on the major surface of the substrate;

(c) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access;

(d) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench;

(e) removing the selectively etched masking layer; and

(f) annealing the trench so that corners at the open and closed ends of the trench become rounded.

7. The method of claim 6, wherein the step of annealing is performed using hydrogen gas.

8. The method of claim 7, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

9. A method of forming a trench in an epitaxial layer of a semiconductor substrate, the trench defined by a closed end at a major surface of the epitaxial layer and a closed end within the body of the epitaxial layer, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the epitaxial layer; and

(b) annealing the trench so that corners at the open and closed ends of the trench become rounded.

10. The method of claim 9, wherein the step of annealing is performed using hydrogen gas.

11. The method of claim 10, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

12. The method of claim 9, wherein the step of annealing also functions to reduce the number of material defects in and/or on the walls of the trench.

13. The method of claim 9, wherein the step of forming the trench is performed using an anisotropic etch.

14. The method of claim 13, wherein, following the annealing step, the width of the trench, away from the rounded ends, remains substantially the same as the width prior to the annealing step.

15. A trench field effect transistor, comprising:

(a) a semiconductor substrate of a first dopant charge type, the substrate embodying the drain of the trench field effect transistor;

(b) a body layer of a second dopant charge type, overlaying a major surface of the substrate;

(c) at least one trench having walls extending through the body layer and into the substrate to a first predetermined depth, the at least one trench having a first end at a major surface of the body layer and a second end at the first predetermined depth;

(d) a dielectric having outer walls adjacent the walls of the at least one trench and inner walls;

(e) a conductor covering the inner walls of the dielectric, the conductor embodying the gate of the trench field effect transistor; and

(f) a pair of source regions of the first dopant charge type, extending from the major surface of the body layer to a second predetermined depth within the body layer and positioned adjacent the outer walls of the dielectric,

wherein corners at both the first and second ends of the at least one trench are rounded as the result of an annealing step applied during the process of fabricating the trench field effect transistor.

16. The trench field effect transistor of claim 15, wherein the anneal step applied during the process of fabricating the trench field effect transistor, is performed using hydrogen gas.

17. The trench field effect transistor of claim 16, wherein the anneal step applied during the process of fabricating the trench field effect transistor, is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

18. The trench field effect transistor ~~of claim~~ 15, wherein during the process of fabricating the trench field effect transistor, the at least one trench is formed using an anisotropic etch.

19. A method of making a trench field effect transistor, comprising:

(a) providing a semiconductor substrate of a first dopant charge type, the substrate embodying the drain of the trench field effect transistor;

(b) growing an epitaxial layer of the same first dopant charge type on the substrate, the epitaxial layer having a different resistivity than the resistivity of the substrate;

(c) forming at least one trench into the epitaxial layer, each trench defined by a first end in a plane defined by a major surface of the substrate and by walls that extend to a second end at a predetermined depth into the epitaxial layer;

(d) annealing the at least one trench to:

(1) reduce the number of defects in the at least one trench created during the step of forming the at least one trench, and

(2) round corners at the first and second ends of the at least one trench;

(e) growing a dielectric layer on the walls of the at least one trench;

(f) forming a conductor over the dielectric layer, the conductor embodying the gate of the trench field effect transistor;

(g) patterning the epitaxial layer and implanting a dopant of a second charge type to form wells interposed between adjacent trenches; and

(h) patterning the epitaxial layer and implanting a dopant of the first charge type to form regions that embody the source regions of the field effect transistor.

20. The method of claim 19, further including the step of forming one or more heavy bodies of the second charge type positioned above the wells and between

the source regions, each heavy body forming an abrupt junction with its corresponding well.

21. The method of claim 19, wherein the step of annealing is performed using hydrogen gas.

22. The method of claim 21, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

23. The method of claim 19, wherein the step of forming the at least one trench is performed using an anisotropic etch.